PRELIMINARY

2,097,152 WORD X 9-BIT RAMBUS DRAM

Description

The TC59R1809VK/HK Rambus DRAM (RDRAM) is next-generation high-speed CMOS DRAM with a 2,097,152-word x 9-bit organization and built-in slave logic. The 36,864 sense amps of the DRAM core are used as cache to achieve data transfer rates of up to 500MB/s. I/O is at the Rambus level, the open drain system being used for output.

The TC59R1809VK/HK uses a 32-pin plastic surface vertical mount package (SVP) enabling a high mounting density, and uses surface horizontal mount package (SHP). Also, the data transfer, which is synchronized with the high-speed clock, the self-refresh function, random access mode function, bit masking, byte masking function and the address mapping function obviate the need for external control circuits, making this DRAM ideal for use in main memory and graphics applications where high performance and low cost are essential.

Features

- Organization
  - RAM: 2,092,152 words x 9 bits (2 banks)
  - Cache: 1024 x 9 x 2 (number of sense amps)
  - Slave Logic
- Self-refresh, Address mapping, and mask-write functions. Random Access Mode, Bit Mask, Byte Mask, Serial Control Packet
- 1K refresh cycles per/32ms
- Package:
  - SVP/SHP
- 3.3V single power supply:
  - 3.3V±0.3V
- IO
  - Rambus™ level

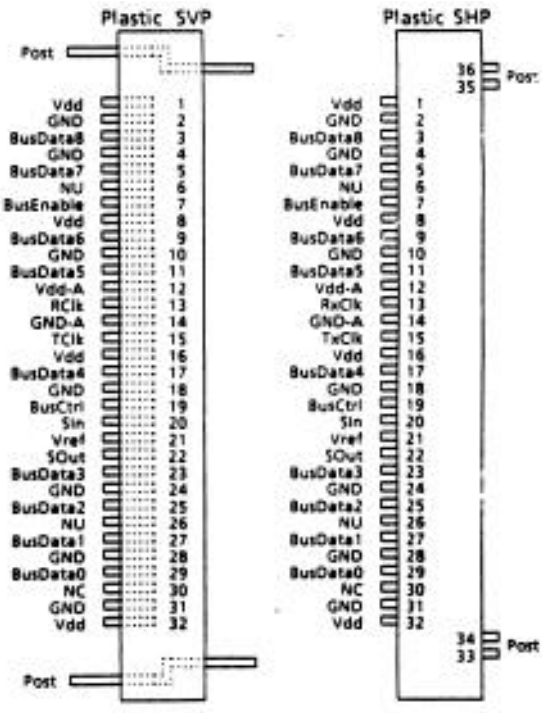
Key Parameters

Main Characteristics			TC59R1809VK
Maximum data transfer rate			2ns
Minimum access time (cache hit)	Writing		16ns
	Reading		40ns
Minimum access time (cache miss)	Dirty Miss	Writing	132ns
		Reading	156ns
Minimum access time (cache miss)	Clean Miss	Writing	100ns
		Reading	124ns
Current consumption			220ns

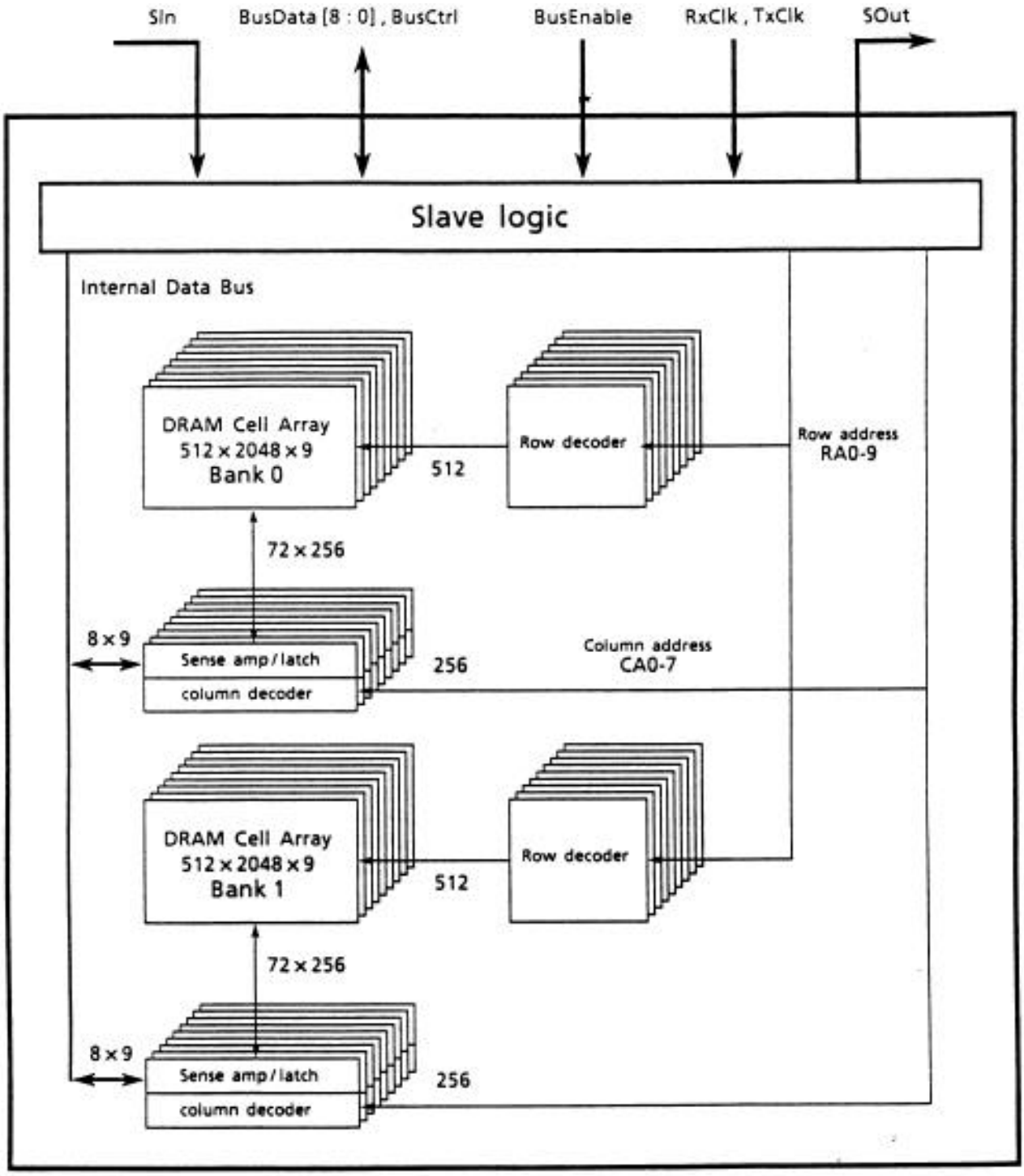
Pin Name

BusData0-8	Bus data I/O
BusCtrl	Bus control I/O
BusEnable	Bus enable input
RClk	High-speed sync clock (for receiving data)
TClk	High-speed sync clock (for sending data)
SIn	Serial signal input
SOut	Serial signal output
Vref	Reference voltage
Vdd/GND	Power supply terminal (+3.3V)/ground
Vdd-A/GND-A	Power supply terminal (+3.3V)/ground (for DLL)
NC	Not connected
NU	Not used (substrate voltage)

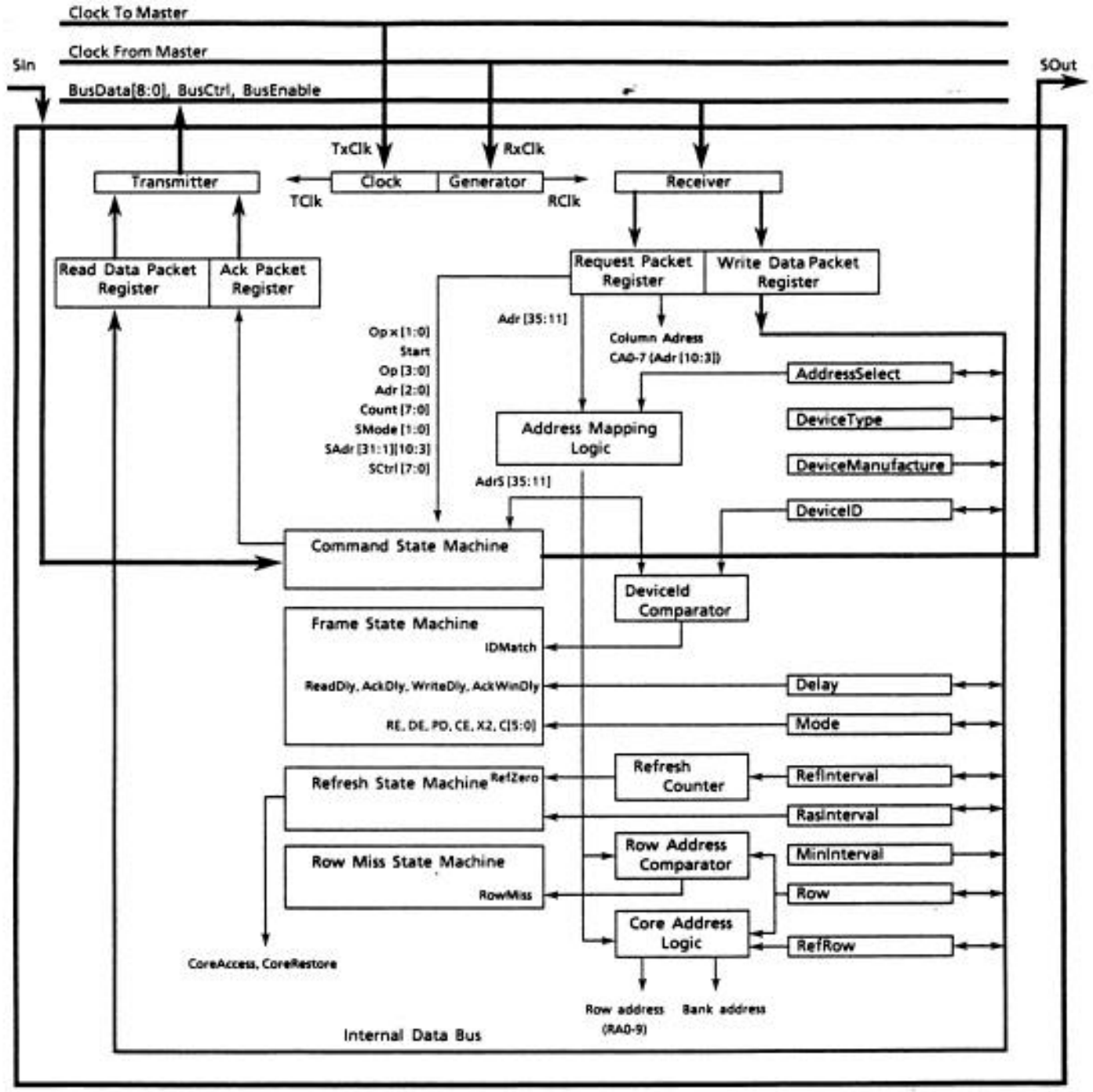
Pin Connection



Internal Block Diagram of RDRAM



Internal Block Diagram of Slave Logic



Maximum Ratings

SYMBOL	ITEM	RATING	UNIT	NOTE
V_{IN}	Input Voltage	-0.5 ~ V_{DD} + 0.5	V	1
V_{IN}	Output Voltage (TTL)	-0.5 ~ 5.5	V	1
Vdd, Vdd-A	Power Supply Voltage	-0.5 ~ 6.5	V	1
T_{OPR}	Operating Temperature	0 ~ 70	°C	1
T_{STG}	Storage Temperature	-55 ~ 125	°C	1
T_{SOLDER}	Soldering Temperature	260	°C	1
P_D	Power Dissipation	3	W	1
I_{OUT}	Output Short-Circuit Current	50	mA	1

Recommended DC Operating Conditions (Ta = 0 ~ 70°C) Note 13

SYMBOL	ITEM	MIN.	TYP.	MAX.	UNIT	NOTE
Vdd, Vdd-A	Power Supply Voltage	3.0	3.3	3.6	V	2
Vref	Reference Voltage	1.9	2.2	2.4	V	2
V_{IH}	High-Level Input Voltage	Vref + 0.35	-	Vref + 0.4	V	2, 13
V_{IL}	Low-Level Input Voltage	Vref - 0.4	-	Vref - 0.35	V	2, 13
V_{IH} (TTL)	High-Level Input Voltage (Sin pin only)	2.0	-	5.5	V	2
V_{IL} (TTL)	Low-Level Input Voltage (Sin pin only)	-0.5	-	0.8	V	2

Capacitance (V_{CC} = 3.3V, f = 1MHz, Ta = 25)

SYMBOL	PARAMETER	MIN	MAX	UNIT
C_I	Input Capacitance (RxClk, TxClk, Busble, Vref)	-	2	pF
C_I (TTL)	Input Capacitance (SIn)	-	10	
C_{IO}	Output Capacitance (BusData[8:0], busCtrl)	-	2	
C_O (TTL)	Output Capacitance (SOut)	-	15	

DC Electrical Characteristics

SYMBOL	ITEM	MIN	MAX	UNIT	NOTE
I_{CC1}	Operating Current	-	220	mA	3, 4, 5
I_{CC2}	Standby Current	-	65		3
I_{CC3}	Refresh Current	-	220		3, 5
I_{CC4}	Mean Operating Current (Typical)	TBD			13
V_{OH}	High-Level Output Voltage	Vref + 0.4	-	V	
V_{OL}	Low-Level Output Voltage	-	Vref - 0.4		
V_{OH}(TTL)	High-Level Output Voltage (SOut only)	2.4	Vdd		
V_{OL}(TTL)	Low-Level Output Voltage (SOut only)	0.0	0.4		
I_{OL}	Output Current (at Low-Level Output)	-	35	mA	6
I_{OH}	Output Current (at High-Level Output)	-10	10	µA	
$I_{I (L)}$	Input Leak Current	-10	10	µA	
$I_{O (L)}$	Output Leak Current	-10	10	µA	
I_{REF}	Vref Current	-10	10	µA	

AC Permissible Operating Conditions and Characteristics

SYMBOL	ITEM	MIN	MAX	UNIT	NOTE
t_{CR}, t_{CF}	Rise Time and Fall Time of TxClk and RxClk	0.3	0.7	ns	7
t_{QR}, t_{QF}	Rise Time and Fall Time of Output Data	0.4	0.6		
t_{CYCLE}	TxClk and RxClk Cycle Times	4	5		
t_{TICK}	Data Transfer Time	0.5	0.5	t_{CYCLE}	8
t_{CH}, t_{CL}	High-Level and Low-Level Time of TClk and RxClk	45%	55%	t_{CYCLE}	
t_{TR}	TxClk-RxClk Differential	0	t_{CYCLE} - 0.6	ns	
t_S	Data Setup Time for RxClk	0.35	-		
t_H	Data Hold Time for RxClk	0.35	-		
t_Q	Data Output Time for TClk	(1-0.4)(t_{CYCLE}/4)	(1-0.4)(t_{CYCLE}/4)		
t_{REF}	Refresh Interval		32	ms	
$t_{LOCK, ACTIVE}$	Lock Time of Interval Clock Generator in ActiveMode		750	t_{CYCLE}	11
$t_{LOCK, STANDBY}$	Lock Time of Interval Clock Generator in StandbyMode		750	t_{CYCLE}	11

RDRAM Access Timing

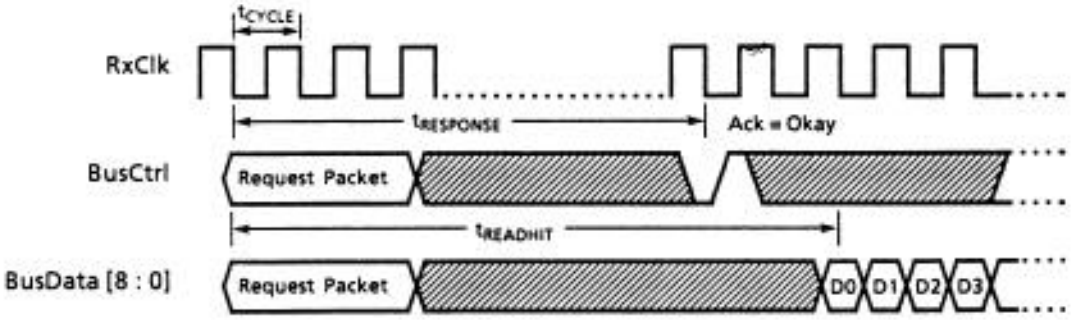
SYMBOL	ITEM	MIN	MAX	UNIT	NOTE
t_{CYCLE}	TxClk and RxClk Cycle-Times	4	5	ns	
$t_{RESPONSE}$	Time from Start Request Packet Start of Read Data Packet (Row Hit)	7	10	t_{CYCLE}	
$t_{READHIT}$	Time from Start Request Packet Start of Write Data Packet (Row Hit)	10	41		
$t_{WRITEHIT}$	Internal between Row Miss and Sending of Next Request Packet	4	35		
$t_{RETRYSENEDCLEAN}$	Start of Request Packet for Row Miss (Nack) to Start of Request Packet for Row Hit. The Previous Row is Unmodified.	21			8
$t_{RETRYSENEDDIRTY}$	Start of Request Packet for Row Miss (Nack) to Start of Request Packet for Row Hit. The Previous Row is Modified.	29			
$t_{READBURST32}$	Time from Start of Request Packet to End 32-Byte Read Data Packet (Row Hit)	26			9
$t_{READBURST256}$	Time from Start of Request Packet to End 32-Byte Read Data Packet (Row Hit)	138			9
$t_{WRITEBURST32}$	Time from Start of Request Packet to End 256-Byte Write Data Packet (Row Hit)	20			10
$t_{WRITEBURST256}$	Time from Start of Request Packet to End 256-Byte Write Data Packet (Row Hit)	132			10
$t_{POSTREGWRITEDELAY}$	Delay from the End of the Current Transaction to the Beginning of the Next Transaction	4			
$t_{POSTMEMWRITEDELAY}$	Delay from the End of the Current Transaction to the Beginning of the Next Transaction	2			
$t_{SERIALREADOFFSET}$	Delay from the Beginning of a Serial Address Sub-packet or a Serial Control Packet	13		t_{CYCLE}	
$t_{SERIALWRITEOFFSET}$	Delay from the Beginning of a Serial Address Sub-packet or a Serial Control Packet to the Beginning of the Read Data Subpacket	5		t_{CYCLE}	

Row Miss and Refresh Parameters

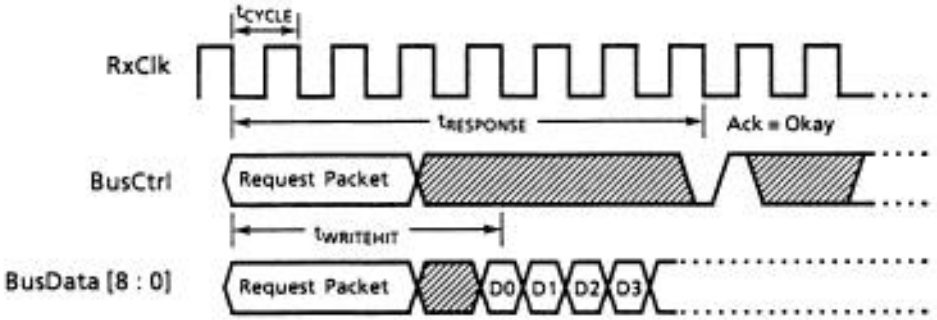
SYMBOL	ITEM	MIN	MAX	UNIT	NOTE
RowOverhead	Overhead Time (Standard Value)	9	-	t_{CYCLE}	
RowPrecharge	Minimum Precharge Time (Standard Value)	9	-	t_{CYCLE}	
RowSense	Rasinterval [1] [4:0] Register	8	-	t_{CYCLE}	
tRAS	RAS Pulse Width	60	-	ns	

Access Timing Chart

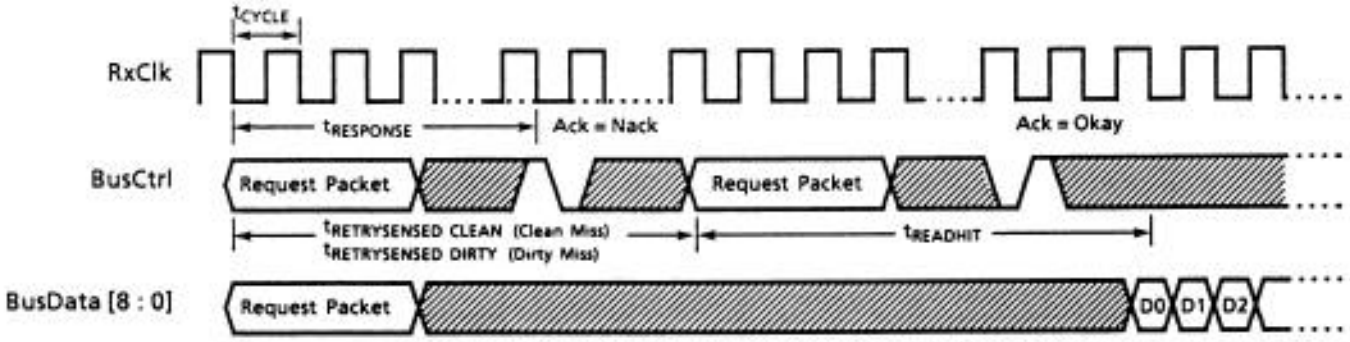
1. Read Timing (Row Hit)



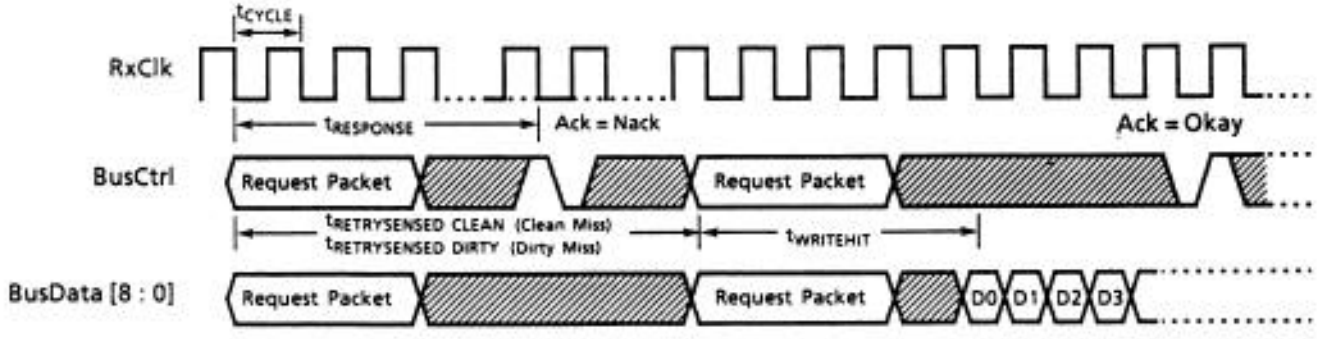
2. Write Timing (Row Hit)



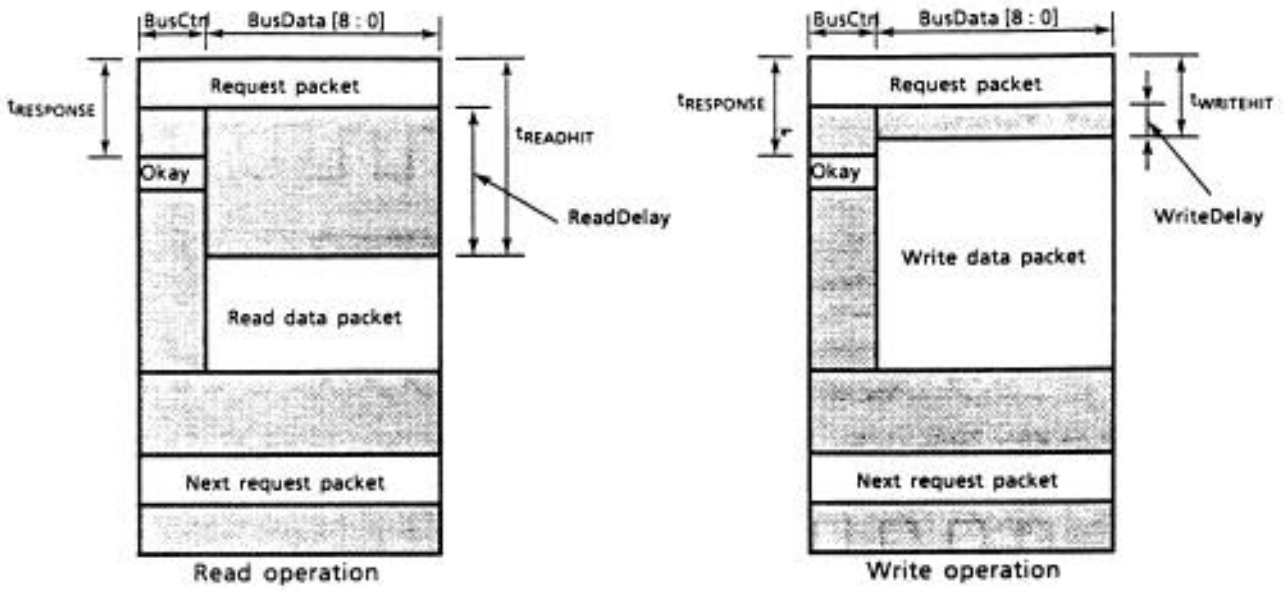
3. Read Timing (Row Miss)



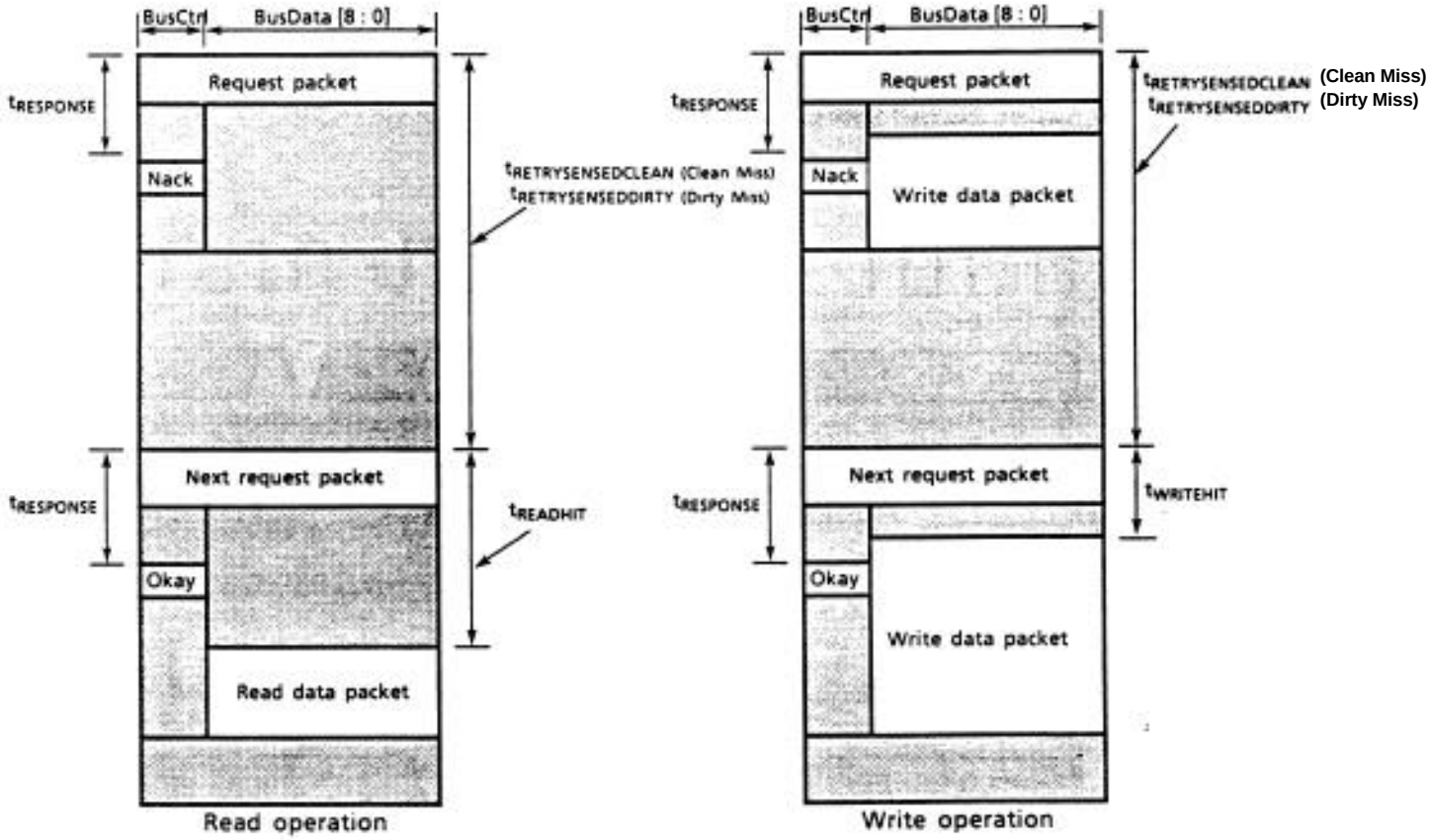
4. Write Timing (Row Miss)



Access Time For Row Sense Amp Cache Miss

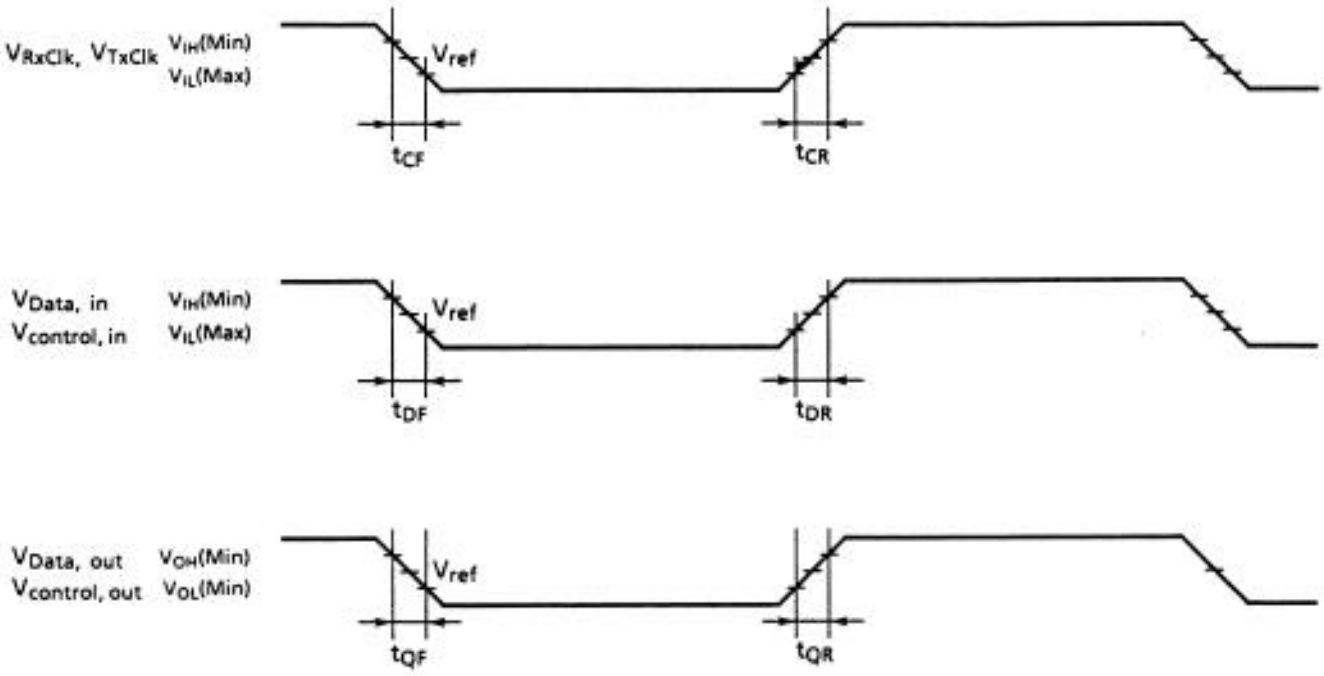


Access Time For Row Sense Amp Cache Hit

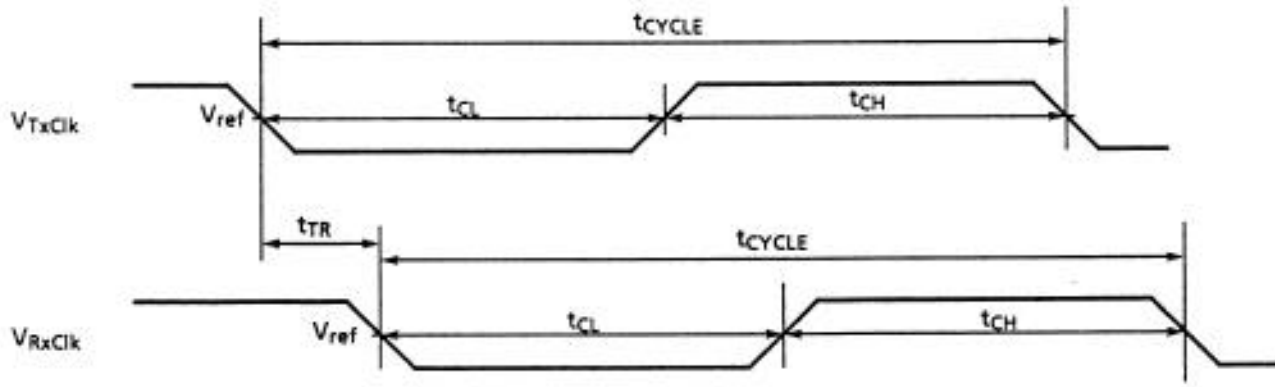


Access Time For Row Sense Amp Cache Miss

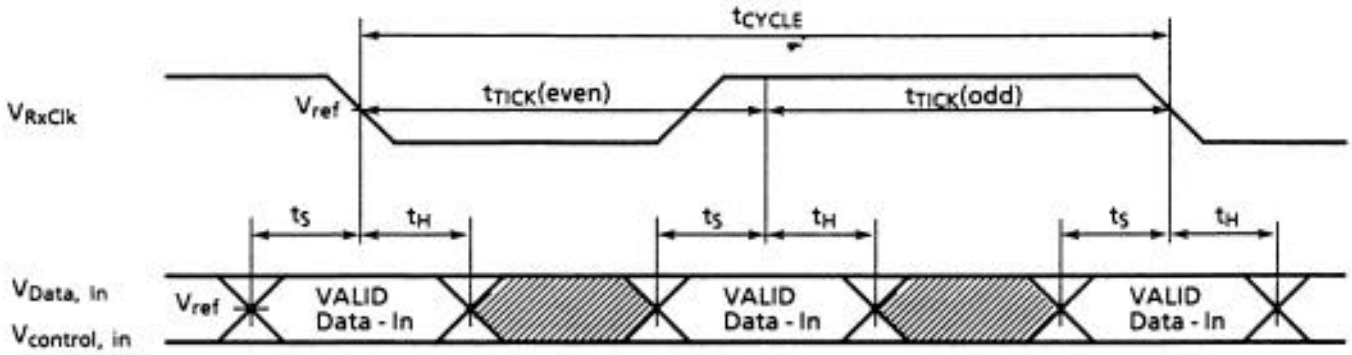
Rise and Fall Timing in I/O Waveform



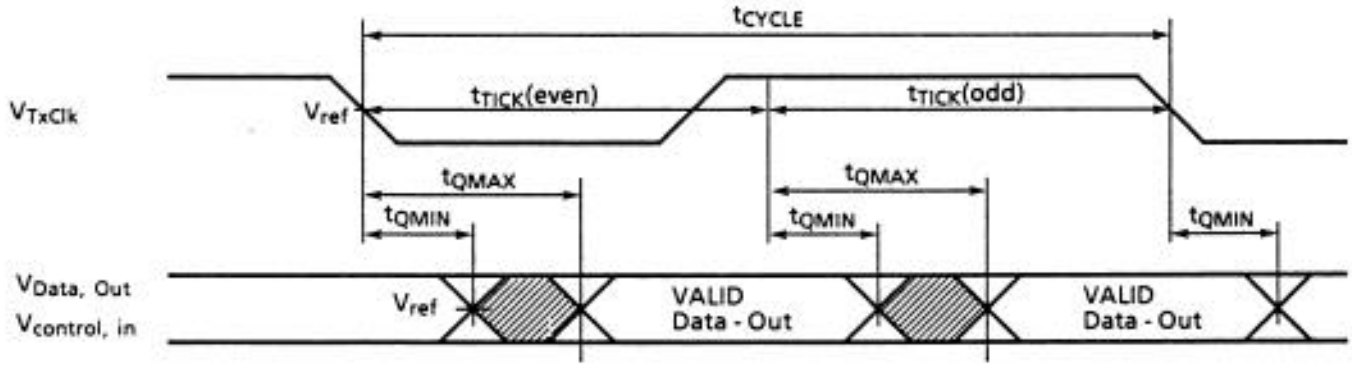
TxClk, RxClk timing



Write Data Set up and Hold Timing for RxClk



Read Data Output Timing for TxClk



Notes:

1. Stress greater than the maximum rated value subject the device to permanent damage.
2. All voltages are given with GND as the reference.
3. These values do not include the BusData [8:0] or BusCtrl output currents.
4. This value is valid when 16 bytes of data are written to memory when the row sense amp cache is hit.
5. These values is valid when t_{CYCLE} = 4ns. They are strongly affected by the value of t_{CYCLE}.
6. The low-level output current is the current when the RDRAM outputs logical level"1". This parameter can be set in the mode register in the slave logic.
7. Vref is used as the reference voltage when measuring the input signal timing.
8. Calculated from the following conditions: t_{CYCLE} = 4ns, and t_{RP} (Min), t_{RP} (Max), and RowOverhead = $2t_{CYCLE}$.
9. Value calculated from $t_{READHIT}$ (Min).
10. Value calculated from $t_{WRITEHIT}$ (Min).
11. These values are 3µs when t_{CYCLE} = 4ns.
12. These values are the average operation current for graphics application systems.
13. Data input swing = Vref +/-0.35V min. Clock input swing = 1 Volt min peak to peak, 425mV min from Vref.

[1] Pin Function

Bus Data I/O: Bus Data [8:0]

This pin is used for inputting request packets and write data packets, and for outputting read data packets. The signal level is referenced to Vref, low-level being logical “1”, high-level being logical “0”.

Bus Control I/O: Bus Ctrl

This pin is used for request packet input and acknowledge packet output. The signal level is referenced to Vref, low-level being “1”, high-level being logical “0”.

Bus Enable Input: Bus Enable

This pin is used for selecting the Rambus DRAM (RDRAM) operating mode (reset, active, standby, or power-down). Transition among the four modes is mainly achieved by varying the length of signal input (pulse width). When no signal is input, standby mode is automatically selected. Active mode is selected with a narrow signal pulse, while reset mode is selected by a wider pulse width. The signal level is referenced to Vref, low-level being logical “1”, high-level being logical “0”.

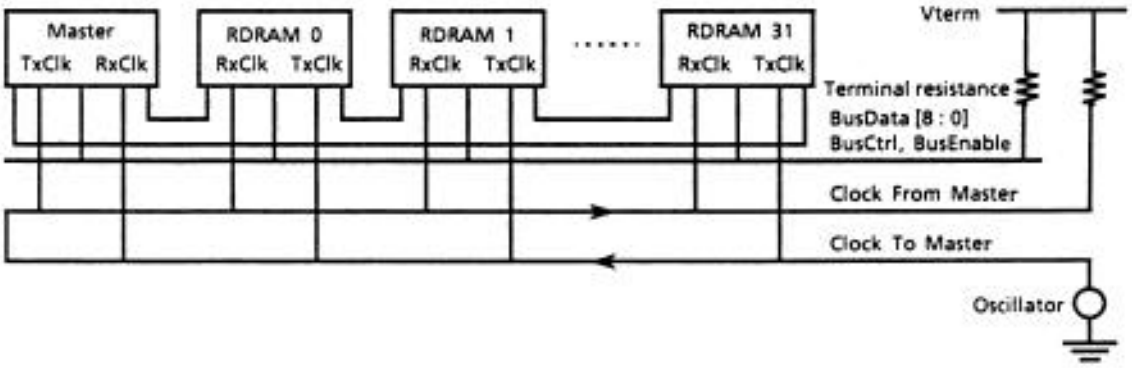


Figure 1. Rambus System Clock

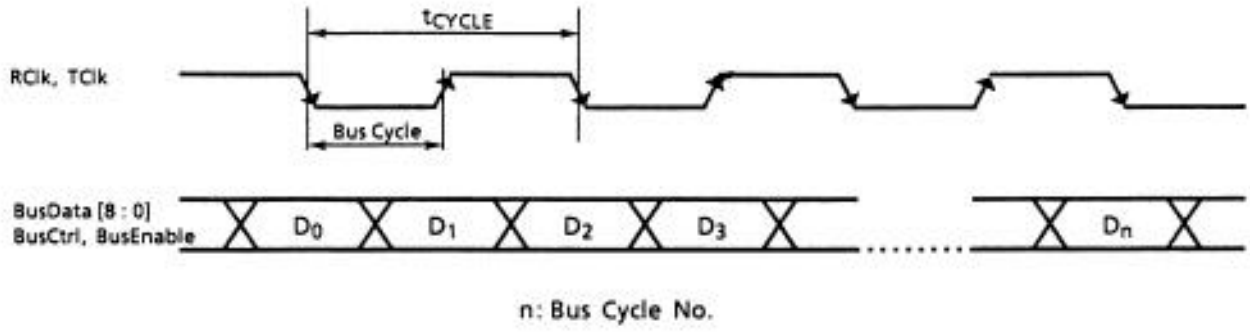


Figure 2. Bus Cycle

High-Speed Sync Clocks: RClk and TClk

These are high-speed sync clocks for input and output data. RClk is used for input data, TClk is used fro output data. In the Rambus system, both clock edges are used for sending data (see Figure 2). The rate between clock edges is known as the bus cycle, with data sent on the trailing edge being known as even bus cycle data and data sent on the leading edge being known as odd bus cycle data. RDRAM access is all referenced to the even bus cycle (trailing edge of clock).

In Rambus systems using RDRAM, skewing between clock signals and data signals must be minimized in order to achieve high-speed data transfer. For this reason, the clock signal line is looped as shown in Figure 1 as the ClockFrom Master and ClockToMaster. In addition, the clock signal line and the data signal line must be arranged in parallel so as to have the same impedance. In Figure 1, the clock traveling from the RDRAM (RDRAM31) at the end of the bus toward the master is known as the ClockToMaster, while that traveling back from the master to the RDRAM is called the ClockFrom-Master. Because ClockToMaster is used as the sync clock when sending data from the RDRAM to the master, ClockTo-Master becomes TClk at the RDRAM and RClk at the master. Vice versa, when data is sent from the master to the RDRAM, ClockFromMaster becomes the sync clock and is TClk at the master and RClk at the RDRAM.

	Master	RDRAM
ClockToMaster	RxClk	TxClk
ClockFromMaster	TxClk	RxClk

The use of this clock system means that the data and clock are always in the same direction, minimizing any skewing between them.

Serial Signal Input and Output: SIn and SOut

These signals are used to initialize the RDRAM and to create the Rambus daisy chain. These signals are the only RDRAM active signals that are CMOS level low-speed signals.

In the Rambus system, each device (RDRAM) must be initialized after powering up. The process of initialization requires the allocation of unique addresses (DeviceID) to each RDRAM in the group. This is achieved continuously using SIn and SOut. SIn and SOut link the whole system as a daisy chain (see Figure 3). In addition to initialization, SIn and SOut are also used for refresh clock input when the RDRAM are in the power-down operating mode. They are not otherwise used in normal operation.

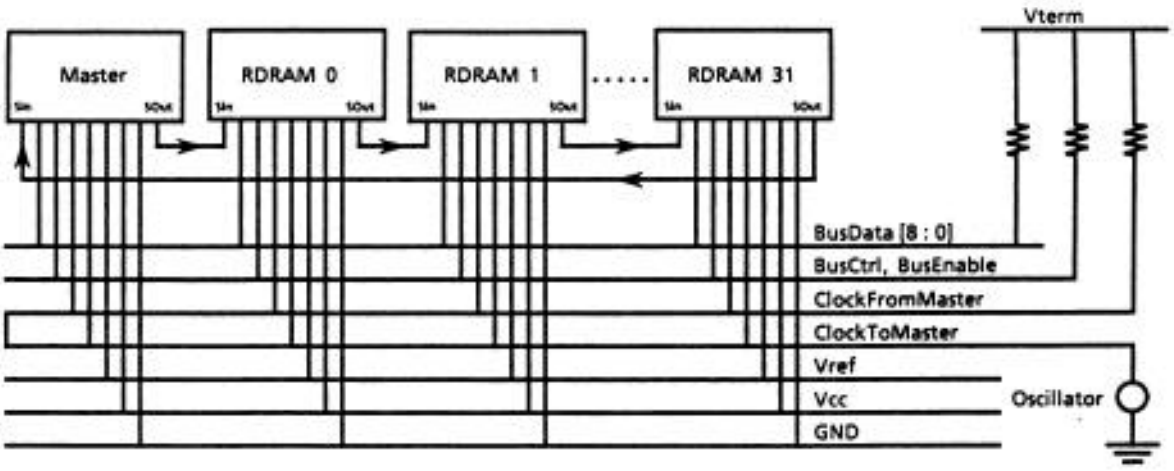


Figure 3. Rambus System

Reference Voltage: Vref

This is reference level for the high-speed small-amplitude signals (BusData [8:0], BusCtrl, BusEnable, RClk, and TClk) used by the RDRAM. When an input signal level is higher than Vref, it is logical “0”; when lower, it is logical “1”.

Post

These pins support the package. They are not electrically connected to the chip

NU (Not Usable)

This pin is connected internally to the lead frame. Because this pin outputs the board potential, do not connect it electrically.

[2] RDRAM Basic Operation

RDRAM access is basically accomplished using request packets, acknowledge packets, and data packets. A packet is a group of contiguous bits sent via the 10 I/O bus lines of BusCtrl and BusData [8:0]. These packets apply the following roles.

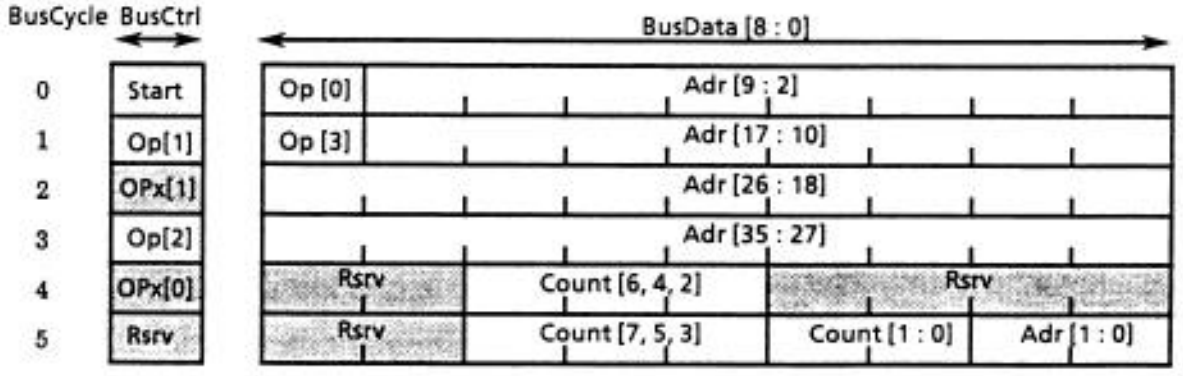


Figure 4. Structure of Request Packet

(1) Request Packet

The request packet is the first packet sent when accessing RDRAM. The request packet, which is made up of 6 cycles X 10 bits of data, includes RDRAM address information, the write/read data packet size, the operation command (to select reading or writing to memory register), and the mask command for the write data. Figure 4 shows the request packet structure.

• Start

The start bit shows the start of a request packet and is logical “1” (low level electrically). Thus, the RDRAM interprets the output of a “1” on the BusCtrl line as the start of a request packet.

• Adr [35:3] (= Address [35:3])

The adr bits show the address requested by the master. As shown in Table 1, the 33-bit address space includes the device ID address and bank address, and the row address and column address.

Table 1. Address Space of Request Packet

	Memory space	Register space
Adr [10:3]	Column address	Register address
Adr [19:11]	Row address	Don’t care
Adr [20]	Bank address	Don’t care
Adr [35:21]	Device ID address	Device ID address

• OP [3:0]/Opx [1:0] (= Operation Command)
These bits select the RDRAM operation command. Table 2 shows the operations for Op [3:0]/OpX [1:0].

Table 2. Operation Commands

Op [3:0]	OpX [1:0]	Name	Description of Operation
0000	00	Rseq	Read sequential data from memory space.
0000	01	Rnsq	Read non-sequential data from memory space.
0100	00	WseqNpb	Write sequential data to memory space with no per-bit mask.
0100	01	WseqDpb	Write sequential data to memory space with data-per-bit masking.
0100	10	WseqBpb	Write sequential data to memory space with both-per-bit masking.
0100	11	WseqMpb	Write sequential data to memory space with mask-per-bit masking.
0110	00	Rreg	Read sequential data from reg. space.
0111	00	Wreg	Write sequential data to reg. space.
1000	00	WnsqNpb	Write non-sequential data to memory space with no per-bit mask.
1000	01	WnsqDpb	Write non-sequential data to memory space with data-per-bit masking.
1000	10	WnsqBpb	Write non-sequential data to memory space with mask-per-bit masking.
1000	11	WnsqMpb	Write non-sequential data to memory space with mask-per-bit masking.
1100	00	WbnsNpb	Write non-sequential data to memory space with byte masking and no per-bit masking.
1100	01	WbnsDpb	Write non-sequential data to memory space with byte masking.
1100	11	WbnsMpb	Write non-sequential data to memory space with byte masking and mask-per-bit masking.
1111		WregB	Broadcast write to reg. space of all responding devices with no acknowledge permitted.

• Count [7:3]
The count bits show the size of the write/read data pack. The oct-byte (OB) unit is used as the unit of data packet size. A value between 1OB (8 bytes) and 32OB (256 bytes) can be specified.

Count [7:3] = 00000 means 1OB, Count [7:3] = 00001 means 2OB, Count [7:3] = 11111 means 32OB.

• Adr [2:0]/Count [2:0]
These bits select master information for the write data. Adr [2:0] and Count [2:0] are the mask information for the first and last OB in the write packet.

• Rsrv (reserved)
These bits are unused. Use the master to set them to”0” when a request is issued.

(2) Acknowledgment Packet

The acknowledgment packet (Ack [1:0]) is the RDRAM response signal request packet. Table 3 shows the meaning of the respective Ack [1:0] signals.

Table 3. Acknowledgment Packet

Ack [1:0]	Command	Description
00	Nonexistent	Nonexistent shows that no RDRAM has the requested address if no output is detected on the BusCtrl line within a set time after the end of the request packet.
01	Okay	Okay shows the completion of receipt of the request packet.
10	Nack	Nack shows that the requested device cannot respond to the request. Nack is output for RDRAM in the case of a row miss or refresh, etc. If a Nack is returned, the master waits before sending the request again.
11	Reserved	Reserved is not currently used. RDRAM does not output Reserved.

(3) Data Packet

The data packet is a group of contiguous write or read data for memory or register address space. The data packet consists of between 1OB (8 bytes) and 32OB (256 bytes). (It is always 1OB when reading or writing to registers.)

(4) Serial Mode Packet

The serial mode packet (SMode [1:0]) controls the state of the Count00 [7:0] and Count11 [7:0] counters. These counters cause operating mode transitions when they reach special values. Figure 5 shows the format of the serial mode packet.

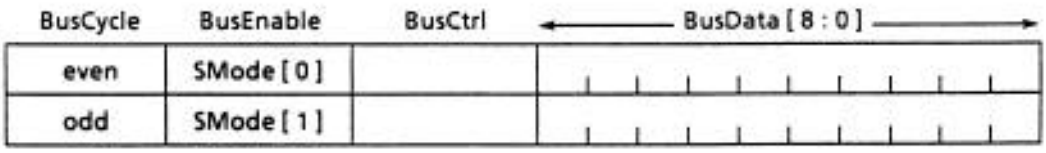


Figure 5. Serial Mode Packet Format

Table 4 shows the meaning of SMode [1:0] signals

Table 4. Serial Mode Fields

SMode [1:0]	Description
00	Increments Count00 [3:0], Clears Count11 [7:0]
01	-
10	-
11	Increments Count11 [7:0], Clears Count00 [3:0]

(5) Serial Address Packet

The serial address packet (SAdr [i] [10:3]) provides eight low-order address bits for each octbyte which is accessed in memory space. These eight address bits are transferred serially on the BusEnable pin on the RDRAM, thus these are called a serial address. This packet is used in random access mode.

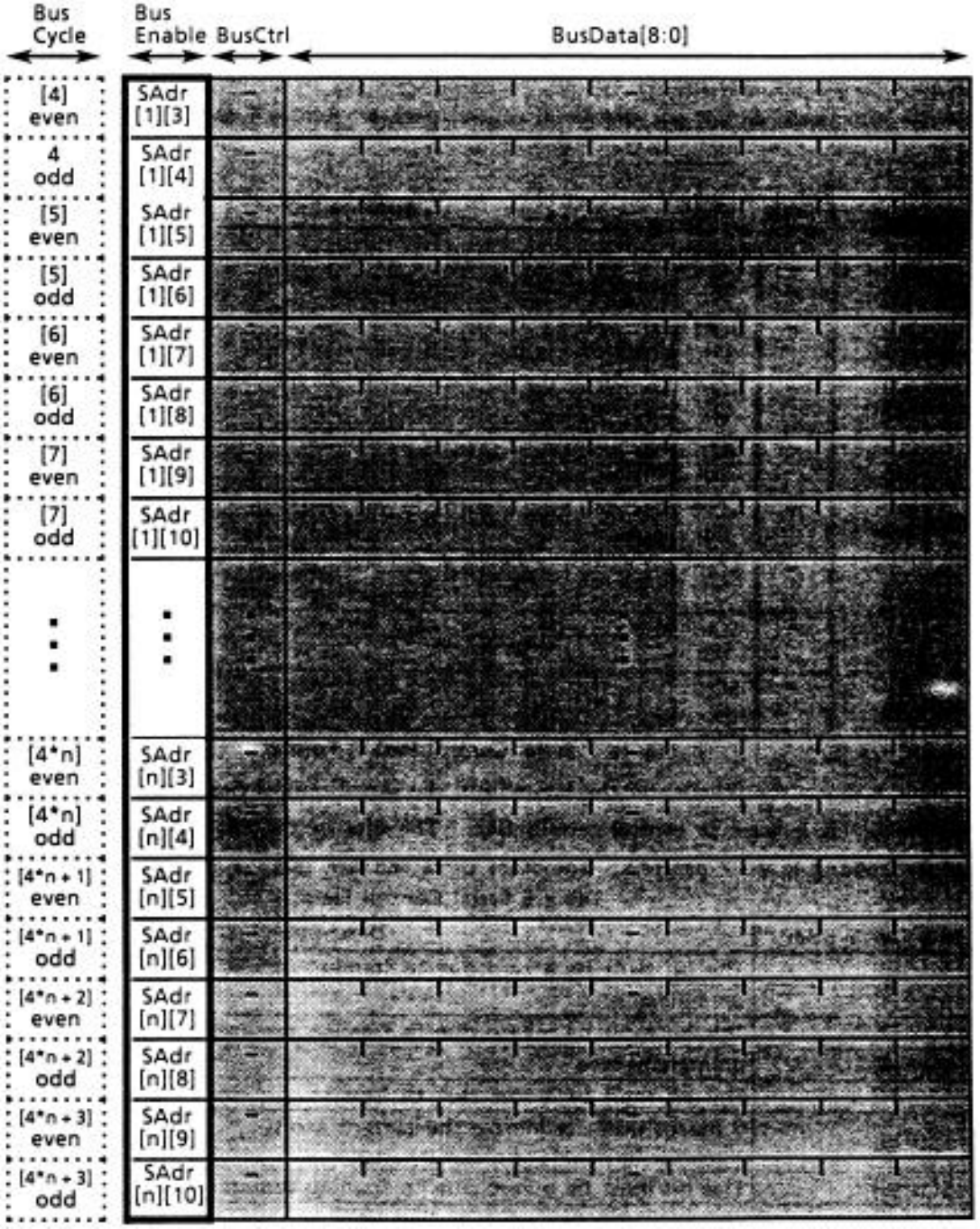


Figure 6. Serial Address Packet Format

Table 5. Serial Mode Fields

Serial Address Fields	Description	
SAdr [i] [10:3]	Low-order address bits for each octbyte	

(6) Serial Control Packet

The serial control packet provides for the early termination of a memory space read or write transaction. It consists of eight bits transferred serially on the BusCtrl pin of the device. The commands which use this packet are all of those which access memory space. The register read and write commands do not use the serial control packet. Figure 7 shows the format of the serial control packet.

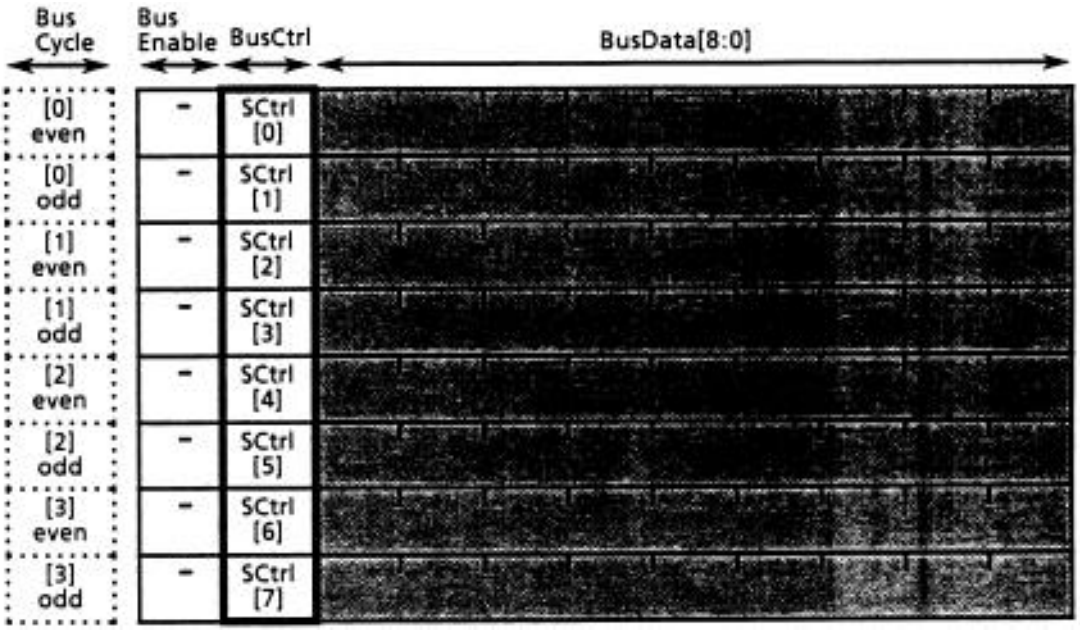


Figure 7. Serial Control Packet Format

Table 6 shows the function of the bits within the serial control fields.

The SCtrl [5] bit is used to control termination. The bits in the even bus ticks must be zero in order for framing to work properly. The other three odd tick bits are unimplemented.

Table 6. Serial Control Fields

Serial Control Fields	Description
SCtrl [0]	This bit must be a zero due to framing requirements
SCtrl [1]	unimplemented
SCtrl [2]	This bit must be a zero due to framing requirements
SCtrl [3]	unimplemented
SCtrl [4]	This bit must be a zero due to framing requirements
SCtrl [5]	0 means do not terminate the current access 1 means terminate the current access
SCtrl [6]	This bit must be a zero due to framing requirements
SCtrl [7]	unimplemented

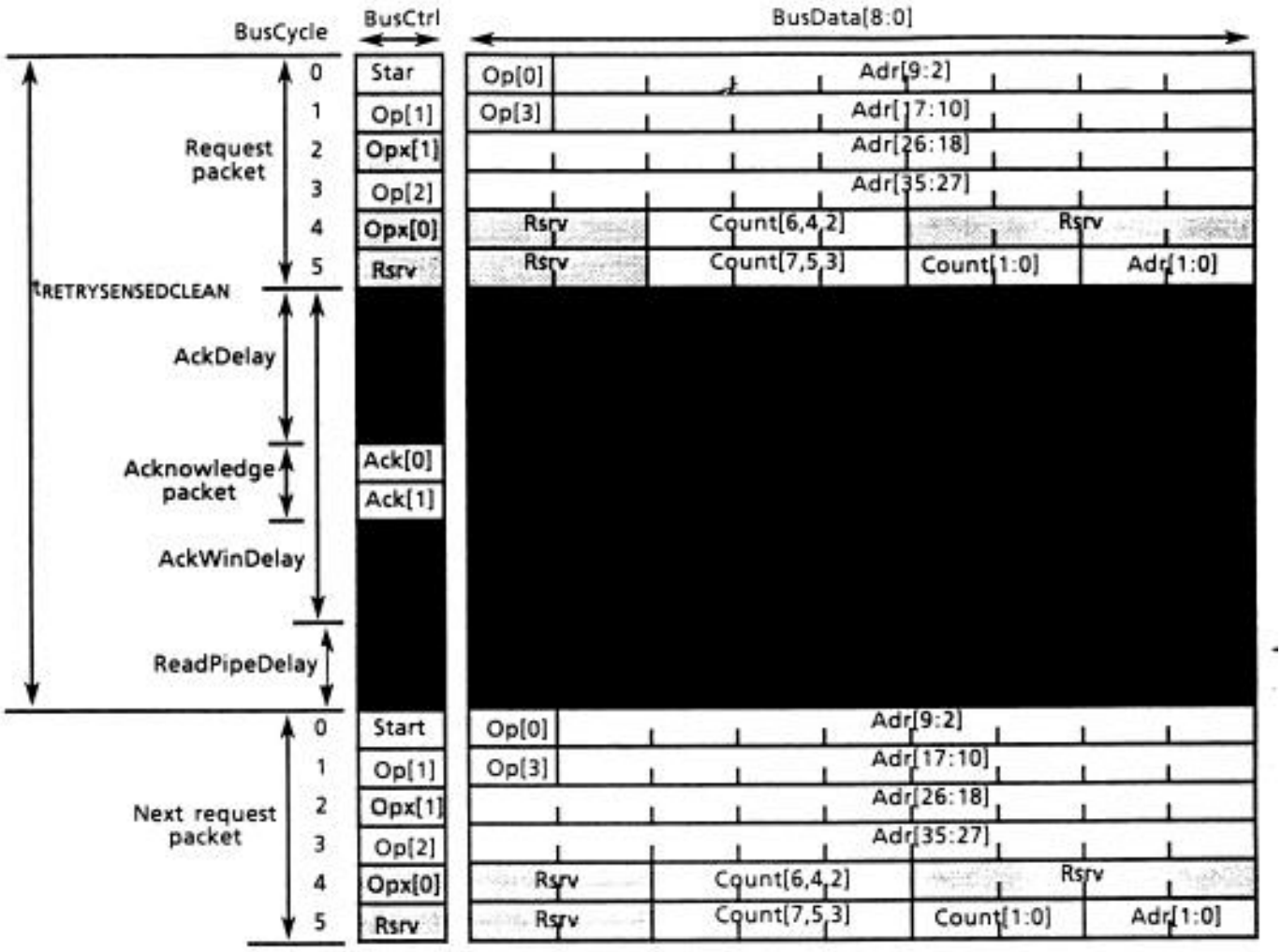


Figure 9. Read Operation for Memory or Register Address Space (Ackpacket = Nack or Nonexistent)

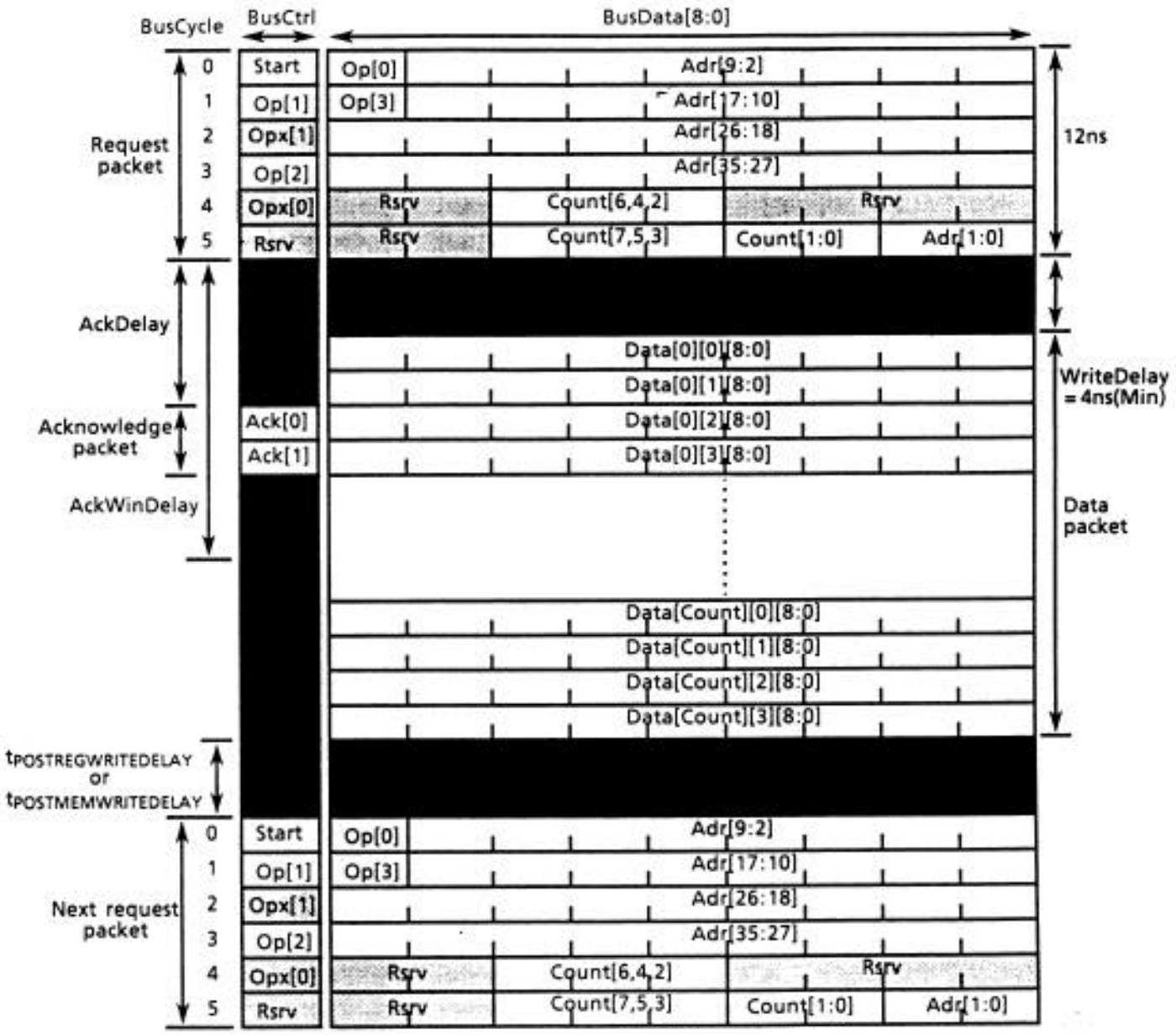


Figure 10. Write Operation for Memory or Register Address Space (Ack packet = Okay)

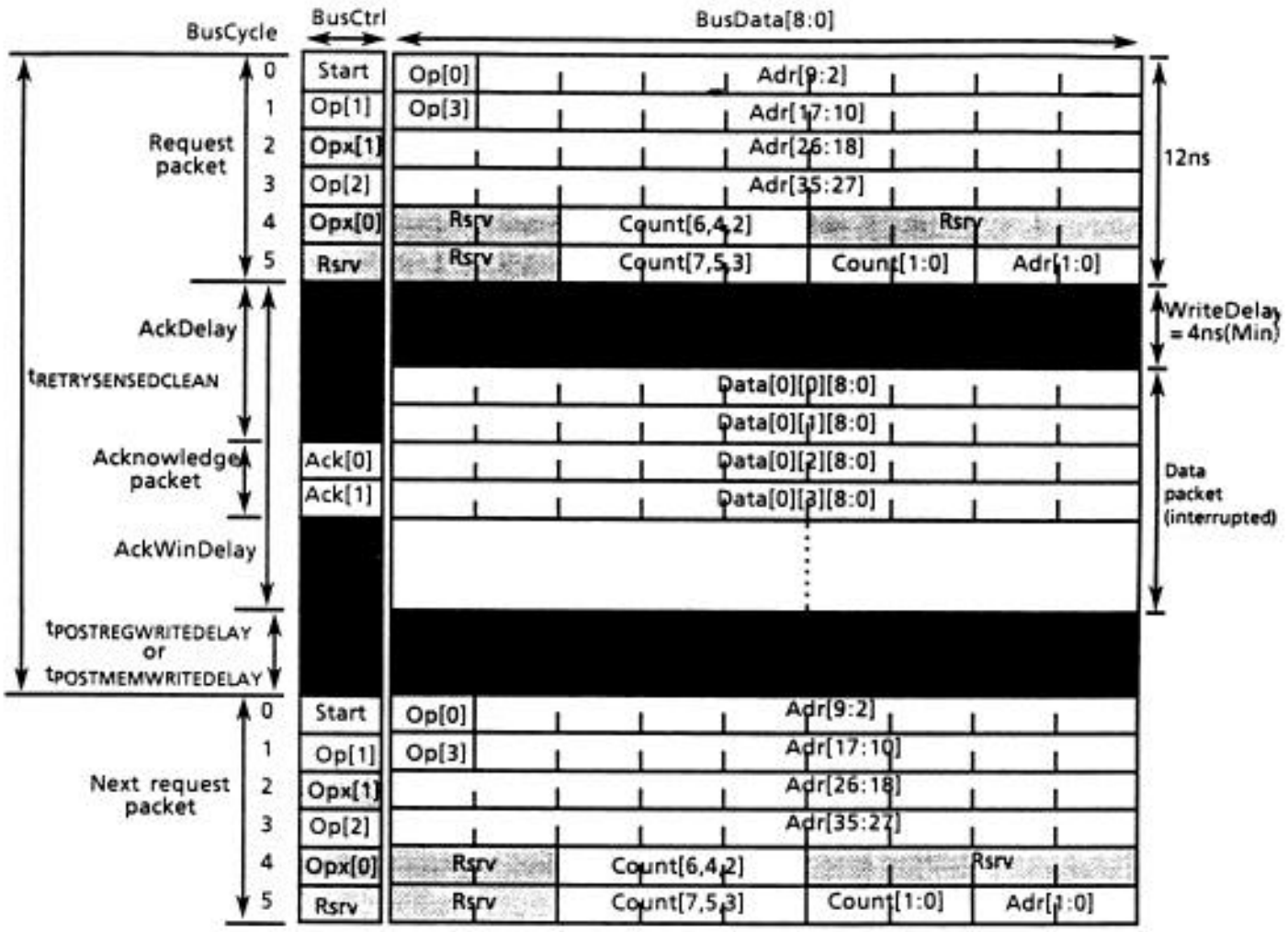


Figure 11. Write Operation for Memory or Register Address Space (Ack packet = Nack or Nonexistent)

[3] Read Operation From Memory or Register

(1) Normal Read Operation

Actual memory or register access using each of the packets is the following. Figure 8 shows the process when a read operation is executed on the RDRAM memory or register space and the RDRAM sends an Okay Ack packet.

RDRAM access with a 6-cycle request packet transmission from the master. The RDRAM detects the request packet from the output (Start bit) on the BusCtrl line. On completion of the request packet, and after AckDelay, the RDRAM outputs a 2-cycle Ack packet.

All devices connected to the Rambus system ignore output on the BusCtrl line for a set interval (AckWinDelay) after the end of the request packet. Therefore, output of the Ack packet cannot be confused with the Start bit of the request packet.

When the RDRAM responds with an Okay Ack packet, the read data packet is output after a delay (ReadDelay) after the end of the request packet. The read operation ends at whichever is last, the end of the AckWindow (AckWinDelay delay after the end of the request packet) or the end of the data packet.

Next, if another operation is to be executed, it starts after a delay of ReadPipeDelay from the end of the pre ceding data packet. (The standard value ReadPipeDelay is $0t_{CYCLE}$.)

The values of AckWinDelay, AckDelay, ReadDelay, and WriteDelay can be programmed by accessing the Delay register in the slave logic.

(2) Read Operations When Nack or Nonexistent is Returned

As Figure 9 shows, no read data packet is output when the RDRAM returns a Nack or Nonexistent Ack packet in a read operation. When the Ack packet is Nack, the RDRAM prepares for another request packet to be sent. The time it takes to prepare depends on the cause of the Nack (row miss or refresh). In the case of a row miss, the preparation time is the time for row precharging ($T_{ROWPRECHARGE}$), row access ($T_{ROWSENSE}$) and RowOverhead. The value of $t_{ROWPRECHARGE}$ and $t_{ROWSENSE}$ can be programmed by accessing the RasInterval register in the slave logic. In the case of a refresh, an additional four cycles are added. During this preparation interval, the RDRAM must wait for the master to output the next request packet.

When the Ack packet is Nonexistent (Ack [1:0] = “00”), (that is, when no output is detected on the BusCtrl line within the AckWindow), either no RDRAM has the requested address or that it was not possible to confirm the requested memory or register space.

(3) Read Operation Commands

Resq : Executes a read operation on RDRAM memory space. The RDRAM configures a read data packet to send to the master

Rreg : Executes a read operation on RDRAM register space. The RDRAM configures a read data packet to send to the master.

[4] Write Operation To Memory or Register

(1) Normal Write Operation

In contrast to read operations, the write data packet is sent from the master before the Ack packet is output, as shown in Figure 10. When another operation is performed immediately after a write operation, it starts after a delay of $t_{POSTRGWRETEDELAY}$ or $t_{POSTMEMWRITEDELAY}$ from the end of the preceeding data packet.

(2) Write Operations When Nack or Nonexistent is Returned (see Figure 11)

In write operation, the write data packet starts to be sent before the Ack packet is output. Therefore, if a Nack or Nonexistent Ack packet is output, the master interrupts the output of the write data packet.

(3) Write Operation Commands

WnsqNpd : Executes a write operation on RDRAM memory space.

Wreg : Executes a write operation on RDRAM register space.

WregB : The RDRAMs can return a Nack, the master is able to confirm that there is a device under internal operation and cannot perform the write operation.

[5] Random Access Mode

In this mode, non-contiguous blocks of memory can be accessed through the use of the read and write non-sequential operations. Using these commands, multiple eight-byte blocks (octbytes) of data within a cache line can be accessed in a non-sequential mode. To do this, the master device sends a request packet specifying a non-sequential operation along with the first octbyte to be accessed.

The master device also generates a serial address packet on the BusEnable signal that specifies the address of the next octbyte. Successive serial address packets continue to specify new addresses in the cache line while data is continuously transferred until the access is complete.

Figure 12 shows a memory space read transaction for a command which uses the serial address packet, and Figure 13 shows a memory space write transaction with a serial address packet.

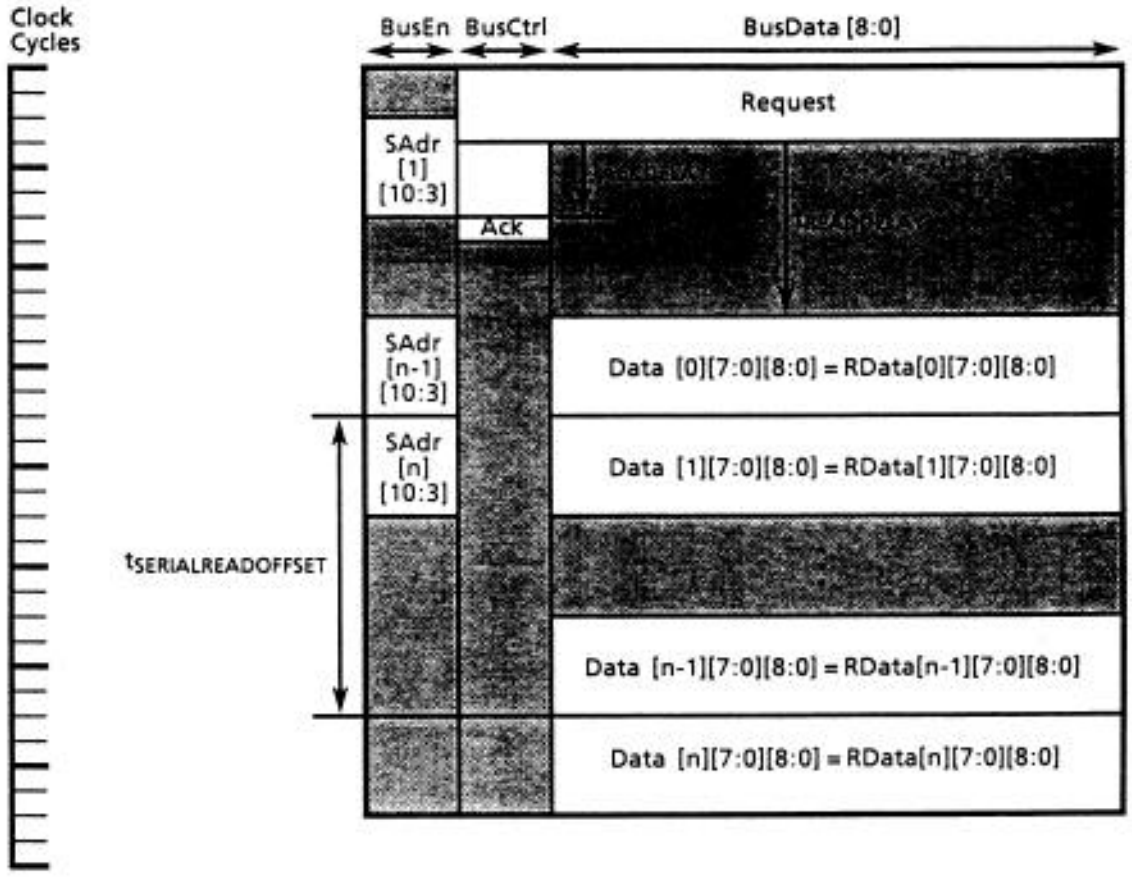


Figure 12. Read Transaction with Serial Address Packet

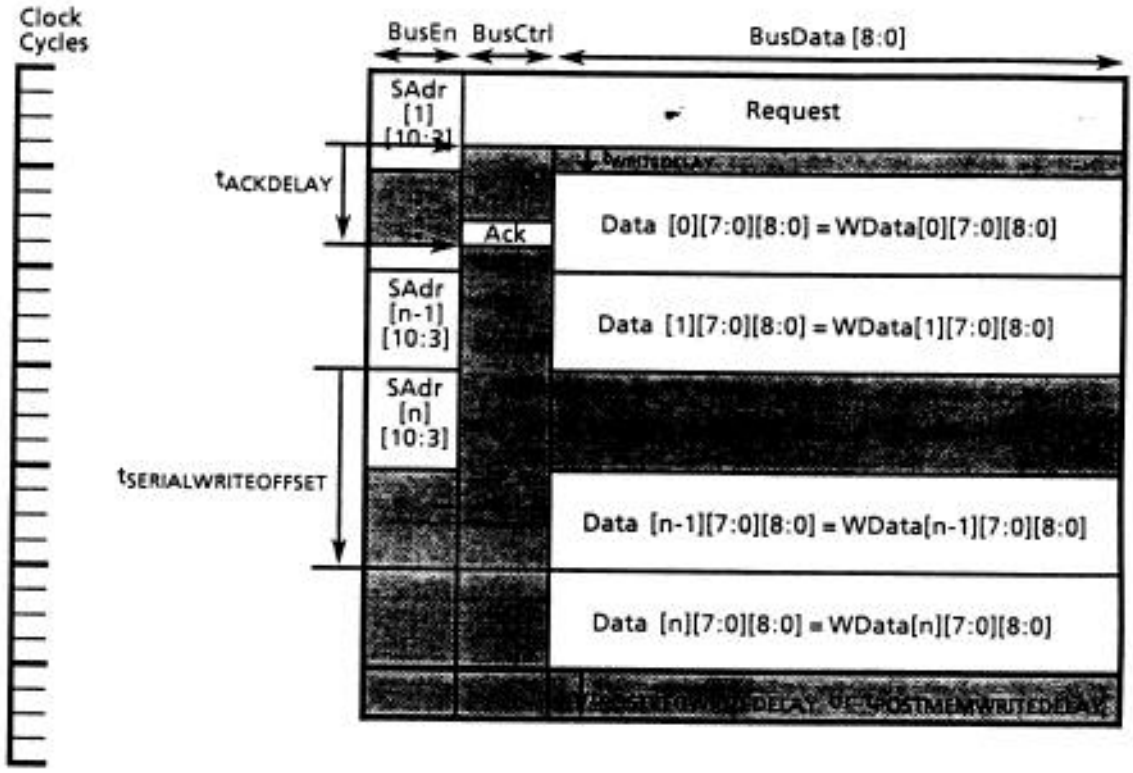


Figure 13. Write Transaction with Serial Address Packet